Ku-BAND MONOLITHIC 2.5-WATT POWER AMPLIFIER FOR HIGH VOLUME APPLICATIONS

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ABSTRACT

The design, tuning, and performance of a 2.5-watt Ku-band power amplifier will be presented. The circuit, which was designed to cover the 16-to 17-GHz band, was modified with some on-chip tuning to correct for unmodeled coupling because of the dense circuit layout and a cross model error in the computer aided design (CAD) program. The on-chip tuning flexibility was then used to achieve 2.5-watt performance in the 14.5-to 16-GHz band for a second amplifier design.

INTRODUCTION

A 2.5-watt Ku-band power amplifier has been designed, built, and tuned to achieve 2-to 2.5-watt performance with power-added efficiencies (PAE) of 18 to 22 percent at 100-percent duty cycle. A device size of 3.7 by 5.2 mm (0.145 by 0.206 inch) allows for the fabrication of 155 circuits on a 3-inch slice. The high efficiency, small size, and standard ion-implanted 0.5-μm GaAs processing allow this amplifier to be well suited for large volume phased array radar applications. Novel on-chip tuning provisions[1] were used to compensate the effects of the unmodeled induced coupling and achieve good performance from 16 to 17 GHz. The on-chip tuning flexibility has also been used to achieve a second design with good performance from 14.5 to 16 GHz.

SINGLE-GATE FET MODELING

A serpentine structure, shown in Figure 1, was chosen as the output FET to achieve reduced temperature operation. Because these FETs generally exhibit 0.4 W/mm power density, an 8-cell output FET with 6,720 μm of gatewidth was chosen. Each cell has 14 gate fingers of 60 μm each. Small-signal S-parameters of 840-μm serpentine FET unit cells and 720-μm conventional FET unit cells, measured at a drain bias of 8 volts and a drain current of 37-percent Idss, were used to create small-signal models for the design of the circuit. The drain voltage of 8 volts was selected as a compromise between optimum power density and gain. The drain current bias of 37-percent Idss was selected based on Texas Instruments experience with high power, high efficiency X-band and Ku-band power amplifiers.

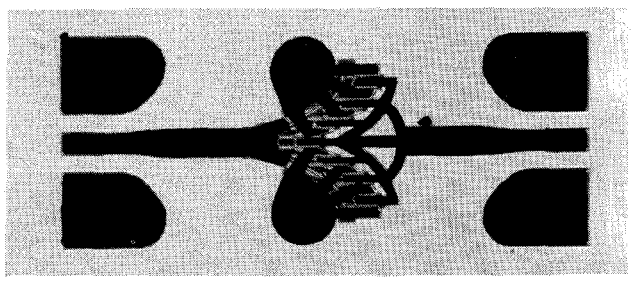

Figure 1. Serpentine Power FET Cell

MONOLITHIC CIRCUIT DESIGN

To achieve the gain goal (16 dB) a three-stage design was required. The output circuit for the 6.72 mm FET was designed using load-line techniques[2]. Second and third harmonic terminations were considered but were not used in order to minimize chip size. At this "almost class A" bias (37-percent Idss) the second harmonic current is only 6 percent of the maximum drain current (Imax) with no other harmonic currents[3]. The size of the second-stage FET (2880 μm) was based on the anticipated large-signal gain of the output FET[3]. The second interstage is designed to present a load-line power match to the second FET. The size of the first FET was selected to be half of the second FET (1440 μm). This device size was selected to ensure good large-signal performance with the first interstage designed for good small-signal performance.

A small resistor (0.4 ohm) in series with the gate of the first FET reduces the transformation ratio to 50-ohms. The input circuit achieves a VSWR of 1.6:1 across the 16- to 17-GHz band in a compact network.

All bias and stabilizing circuitry are on-chip to save space and reduce parts count in system integration. Ground points adjacent to the RF bonding pads allow for on-wafer RF characterization and screening to increase system yield. A photograph of the original circuit is shown in Figure 2.

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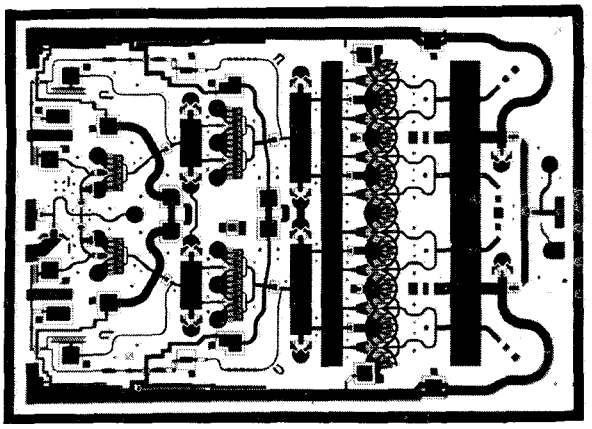

Figure 2. Ku-Band Power Amplifier

The Ku-band Power Amplifier circuit uses "optimum-microstrip-interconnects" to help absorb the bond wire inductance at the RF input and output of the device. This scheme uses a flared, capacitive bond pad on the 50-ohm transmission line (line) and a large 300- by 120-μm (12 by 4 mil) capacitive bond pad on the MMIC. The two shunt capacitances of the bond pads connected with the bond wire inductance forms a Pi-filter section. This interconnect scheme reduces the sensitivity to bond wire length (compared to the 50 ohm line without flares) and will increase system yield in a high volume automated assembly environment.

LAYOUT CONSIDERATIONS FOR CIRCUIT FLEXIBILITY

Circuit flexibility involves being able to change the electrical characteristics of the tuning structures that make up the circuit. These changes are often needed to achieve the full potential of the circuit. Modeling errors, CAD errors, and the unmodeled effects of coupling because of a dense circuit layout can cause the measured and predicted circuit performance to differ.

Lines with impedances of 23 to 80 ohms are used in the design of this circuit. The length of a line is the easiest parameter to vary in the laboratory. A longer line can be realized by removing an air-bridge and rerouting the line to a longer path with bond wires[1]. Lines with bends can be shortened by shortcutting the corner with a bond wire.

In this circuit design, 17 shunt capacitors are used. Where there is extra space, two additional shunt capacitors with bond pads were added but not connected in the original design. An 18-percent smaller capacitor (smaller than the one in the circuit) and an 18-percent larger capacitor allow some shunt capacitance tuning flexibility.

UNTUNED PERFORMANCE

The small-signal gain of the original circuit fell 2 to 5 dB short of the predicted performance, as shown in Figure 3. The input return loss was 10 to 15 dB compared to a predicted return loss greater than 20 dB, as shown in Figure 4.

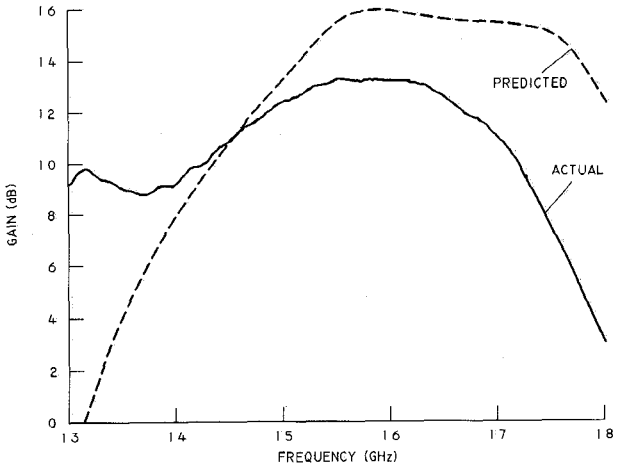

Figure 3. Actual Versus Predicted Small Signal Gain

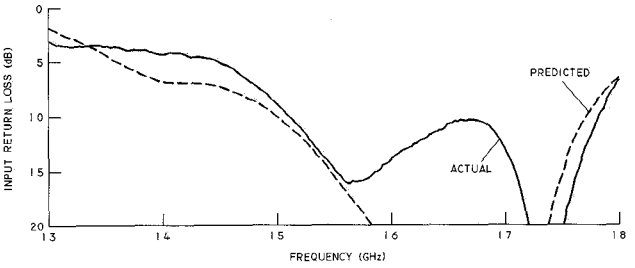

Figure 4. Actual Versus Predicted Input Return Loss

The output circuit is laid out to minimize undesired coupling. This was a chip-size compromise to achieve a bandwidth greater than 10 percent, output power greater than 2 watts, and PAE greater than 22 percent. All goals and data presented are CW (100-percent duty cycle) at room temperature. The output power and efficiency fell short of the goals, as shown in Figure 5. This shortfall was traced to a poor cross model in the version of the CAD tool used. Newer versions of the CAD tool used and another CAD tool confirmed the cross model problem. Crosses occur in every section of the amplifier.

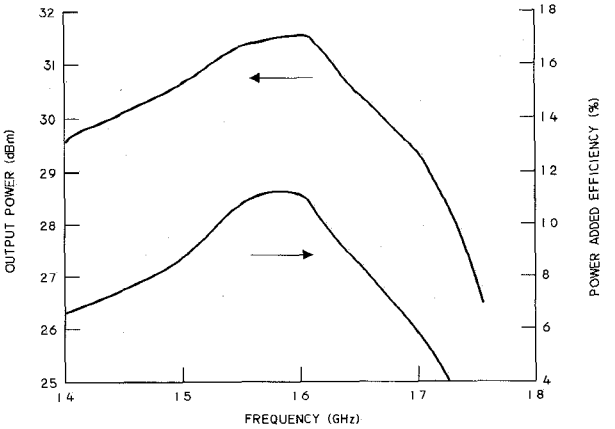

Figure 5. Untuned Output Power and Efficiency

CIRCUIT ENHANCEMENT FOR UPPER Ku-BAND

On-chip tuning provisions were used to correct the shortfalls discussed in the previous section. Tuning yielded the 2 to 2.5 watts desired with PAE exceeding 20 percent for most of the band. The tuned amplifier performance is illustrated in Figure 6. Tuned small-signal gain exceeds 18 dB and the input return loss exceeds 17 dB, as shown in Figure 7.

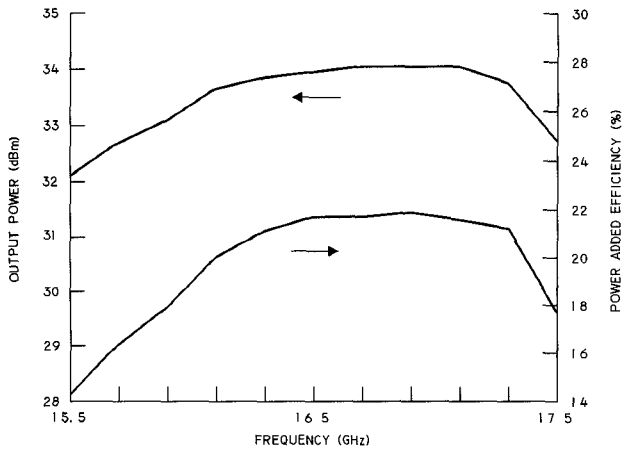

Figure 6. Output Power and Efficiency for Upper Ku-Band

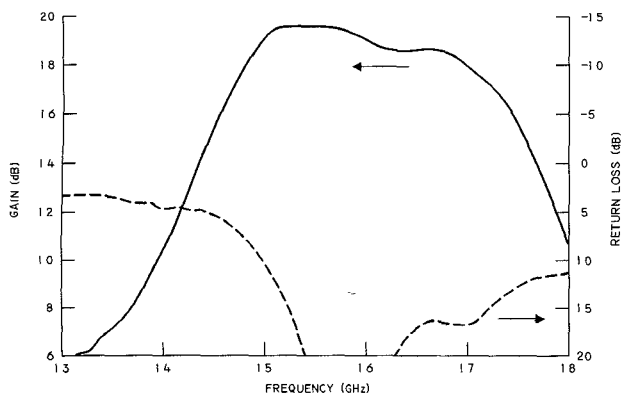

Figure 7. Small-Signal Gain and Input Return Loss for Upper Ku-Band

Second iteration devices exhibit small-signal gain exceeding 17 dB and input return loss exceeding 13 dB as shown in Figure 8, and an output power of 2.5 watts at 25-percent PAE as shown in Figure 9.

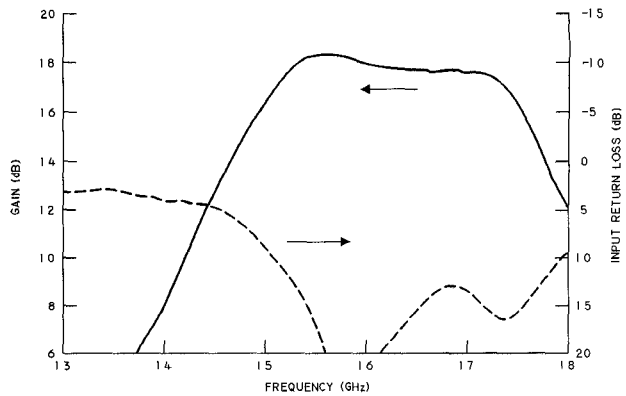

Figure 8. Second Iteration Small-Signal Gain and Input Return Loss

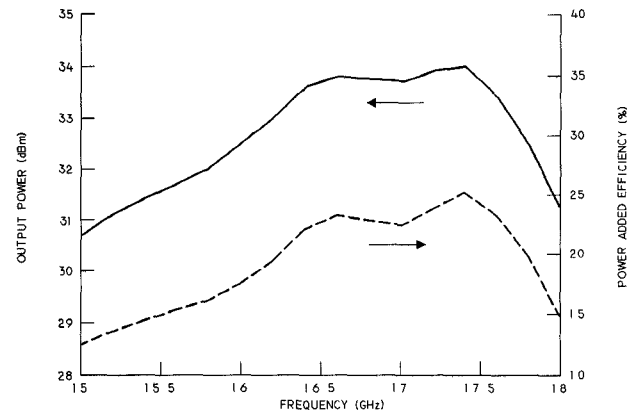

Figure 9. Second Iteration Output Power and Efficiency

CIRCUIT ENHANCEMENT FOR MIDDLE Ku-BAND

To cover an additional application the amplifier was tuned to the 14.5- to 16-GHz band. The first circuit was tuned to achieve 16 dB of gain and 7 to 18 dB of input return loss, as shown in Figure 10. This tuning was added to a circuit on a carrier plate with our 5-stage driver amplifier circuit, as shown in Figure 11. This carrier plate with -3 dBm applied exhibits 2 to 2.5 watts with PAE of 20 to 22 percent from 14.5 to 16 GHz (CW, room temp.) in Figure 12.

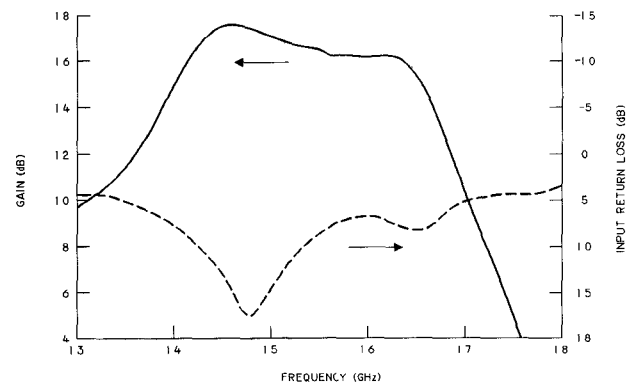

Figure 10. Small-Signal Gain and Input Return Loss for Middle Ku-Band

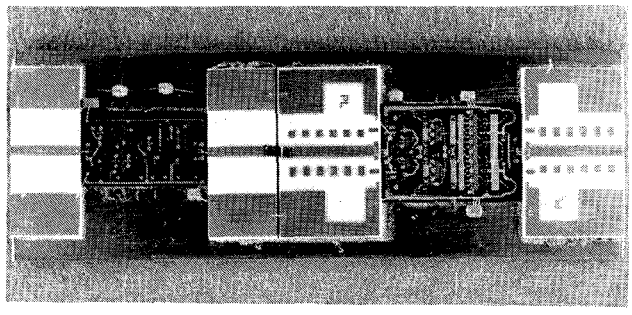

Figure 11. Ku-Band Power Amplifier with Driver Amplifier

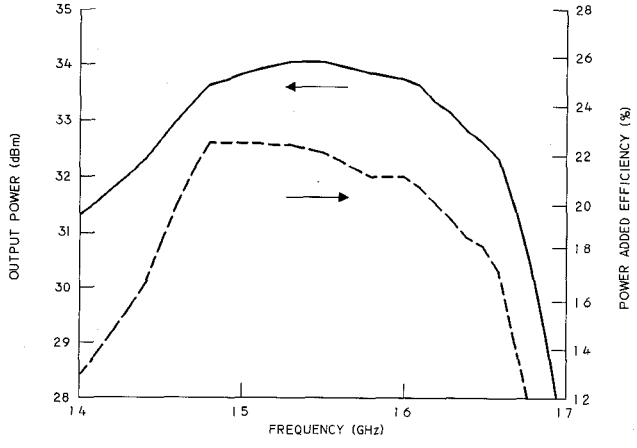

Figure 12. Output Power and Efficiency of Driver/Power Amplifier at Middle Ku-Band

CONCLUSION

Two successful designs were achieved without multiple full-up mask set redesigns or large GaAs inefficient layouts that avoid all undesired coupling. Four new mask levels allow the original mask set to produce successful parts. Another four mask levels will allow good performance in an adjacent frequency band. This approach yields small (lower cost) densely packed successful circuits.

ACKNOWLEDGEMENTS

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3. L.J. Kushner, "Microwave Power Amplifier Analysis and Design" Massachusetts Institute of Technology Lincoln Laboratory, Technical Report 812, 16 December 1988.